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An approach to reducing complexity of neuromorphic fault dictionary construction for analogue integrated circuits

Mosin S.
Kazan Federal University, 420008, Kremlevskaya 18, Kazan, Russia

Abstract

© 2018 IEEE. This paper is mainly focused on the reducing a complexity of fault dictionary constructing for analog integrated circuits based on neural network. The benefits of fault dictionary based on neural network (NN) such as associative operating mode and small influence of the number of considered faults on the NN architecture are presented. The problems of constructing the neuromorphic fault dictionary in the aspect of big data are discussed. The approach to selection the essential characteristics of controlled parameters during testing and fault diagnostics as well as to reduction of the training set dimension is proposed. The principal component analysis (PCA) and criterion based on the explained residual variance are applied for reduction the number of coefficients used for the neural network training. The decomposition of design flow corresponding to the proposed approach is presented. The experimental results demonstrates efficiency as the time and computational cost reduction for the construction of neuromorphic fault dictionary, which provides high fault coverage up to 100 %.

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Keywords

Analog circuits, Design-for-testability, Neuromorphic fault dictionary, Principal component analysis, Testing and diagnostics

References

[1] S. Mosin, "Design-for-testability automation of mixed-signal integrated circuits, " 2013 IEEE International SOC Conference, Erlangen, 2013, pp. 244-249.

[2] P. N. Variyam and A. Chatterjee, "Specification-driven test design for analog circuits, " Proceedings 1998 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (Cat. No. 98EX223), Austin, TX, 1998, pp. 335-340.

[3] S. Mosin, "A technique of analog circuits testing and diagnosis based on neuromorphic classifier, " Advances in Intelligent Systems and Computing, Vol. 425, 2016, pp. 381-393.

[4] S. Mosin, "Automated simulation of faults in analog circuits based on parallel paradigm, " 2017 IEEE East-West Design & Test Symposium (EWDTS), Novi Sad, 2017, pp. 1-6.

[5] C. Zhang, G. He and S. Liang, "PCA-Based Analog Fault Detection by Combining Features of Time Domain and Spectrum, " 2009 International Workshop on Intelligent Systems and Applications, Wuhan, 2009, pp. 1-4.

[6] G. He, C. J. Zhang, G. H. Chang, S. H. Liang, 'Testing Analog Circuits by PCA of Power Supply Current", Applied Mechanics and Materials, Vol. 157-158, 2012, pp. 641-645.

[7] J. Xiong, S. Tian, and C. Yang, "Fault Diagnosis for Analog Circuits by Using EEMD, Relative Entropy, and ELM", Computational Intelligence and Neuroscience, 2016, Article ID 7657054, 9 p.

[8] B. Long, M. Li, H. Wang, and S. Tian, "Diagnostics of analog circuits based on LS-SVM using time-domain features, " Circuits, Systems, and Signal Processing, vol. 32, no. 6, pp. 2683-2706, 2013.

[9] M. Aminian, F. Aminian, "Neural-network based analog circuit fault diagnosis using wavelet transform as preprocessor", IEEE Trans. CAS II, Vol. 47, Feb. 2000, pp. 151-156.

[10] L. Yuan, Y. He, J. Huang, and Y. Sun, "A new neural-network-based fault diagnosis approach for analog circuits by using kurtosis and entropy as a preprocessor, " IEEE Transactions on Instrumentation and Measurement, Vol. 59, No. 3, 2010, pp. 586-595.

[11] I. T. Jolliffe, Principal Component Analysis. Springer, 2002, 488 p.